CLAIMS

Please cancel claims 25, 50, and 56 without prejudice or disclaimer.

Please amend the claims as shown in the following claim listing.

1. (Currently amended) A method comprising:

checking a current clock period when a memory is accessed ~~to read data~~, the current clock period being one of a given number of clock periods; and

setting a usage bit corresponding to the current clock period during a writeback cycle to write ~~the read~~ data read from the memory back to the memory, the usage bit indicating usage information for the ~~read~~ data.

2. (Currently amended) The method of claim 1, ~~further~~ comprising:

erasing usage bits corresponding to a new clock period.

3. (Previously presented) The method of claim 2, wherein erasing includes erasing usage bits at once.

4. (Currently amended) The method of claim 1, ~~further~~ comprising:

resetting usage bits in response to changing an ~~address/tag of the memory~~address or tag for the memory; and

setting a usage bit corresponding to a current clock period.

5. (Original) The method of claim 1, wherein the memory is a non-volatile cache memory.

6. (Previously presented) The method of claim 1, wherein the given number of clock periods is four.

7. (Canceled).

8. (Previously presented) The method of claim 1, wherein the memory is a destructive read memory.

9. (Original) The method of claim 8, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

10. (Canceled).

11. (Currently amended) The method of claim 1, ~~further~~ comprising:

de-allocating data in the memory based upon usage bits.

12. (Currently amended) A memory comprising:

an area to store data; and

an area to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for ~~data~~entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding ~~to~~ one of a given number of clock periods,

wherein the memory is a destructive read memory and wherein a usage bit for ~~data~~an entry read from the memory is to be updated during a writeback cycle to write the read ~~data~~entry back to the memory.

13. (Original) The memory of claim 12, wherein the usage information is a least recently used information.

14. (Previously presented) The memory of claim 12, wherein the destructive read memory is a cache memory.

15. (Previously presented) The memory of claim 12, wherein the given number of clock periods is four.

16. (Canceled).

17. (Previously presented) The memory of claim 12, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

18. (Currently amended) A system comprising:

a magnetic memory device;

a destructive read memory to cache data for the magnetic memory device and to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for ~~data~~entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding ~~to~~ one of a given number of clock periods; and

a memory controller to update a usage bit for ~~data~~an entry read from the memory during a writeback cycle to write the read ~~data~~entry back to the memory, the memory controller to de-allocate ~~data~~an entry using ~~the plurality of~~ usage bits.

19. (Original) The system of claim 18, wherein the usage information is a least recently used information.

20. (Previously presented) The system of claim 18, wherein the destructive read memory is a non-volatile cache memory.

21. (Previously presented) The system of claim 18, wherein the given number of clock periods is four.

22. (Canceled).

23. (Currently amended) A method comprising:

storing ~~metadata comprising~~usage bits to indicate usage information for ~~data~~entries in a memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods; and

updating ~~usage information~~a usage bit for ~~data~~an entry read from the memory during a writeback cycle to write the read ~~data~~entry back to the memory.

24. (Original) The method of claim 23, wherein the usage information is a least recently used information.

25. (Canceled).

26. (Currently amended) The method of claim ~~25~~23, wherein updating a usage ~~information~~bit comprises:

checking a current clock period when the memory is accessed ~~to read data~~, the current clock period being one of a predetermined number of clock periods; and

setting a usage bit corresponding to the current clock period~~, the usage bit indicating usage information for the read data~~.

27. (Previously presented) The method of claim 26, comprising:

erasing usage bits corresponding to a new clock period.

28. (Currently amended) The method of claim 26, comprising:

resetting usage bits when an ~~address/tag of the metadata~~address or tag for an entry is changed; and

setting a usage bit corresponding to a current clock period.

29. (Previously presented) The method of claim 23, wherein the memory is a non-volatile cache memory.

30. (Previously presented) The method of claim 26, wherein the predetermined number of clock periods is four.

31. (Previously presented) The method of claim 23, wherein the memory is a destructive read memory.

32. (Currently amended) A machine readable medium having executable instructions comprising:

a first group of executable instructions to check a current clock period when a memory is accessed ~~to read data~~, the current clock period being one of a predetermined number of clock periods; and

a second group of executable instructions to set a usage bit corresponding to the current clock period during a writeback cycle to write ~~the read~~ data read from the memory back to the memory, the usage bit indicating usage information for the ~~read~~ data.

33. (Currently amended) The medium of claim 32, ~~further~~ comprising:

a third group of executable instructions to erase usage bits corresponding to a new clock period.

34. (Currently amended) The medium of claim 32, ~~further~~ comprising:

a third group of executable instructions to reset usage bits ~~for the memory~~ in response to changing an ~~address/tag of the memory~~address or tag for the memory, and to set a usage bit corresponding to a current clock period.

35. (Currently amended) A machine readable medium having executable instructions comprising:

a first group of ~~computer~~executable instructions to store ~~metadata information for data~~usage bits to indicate usage information for entries in a memory, ~~wherein the metadata~~

~~information includes usage information~~a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods; and

a second group of ~~computer~~executable instructions to update ~~usage information~~a usage bit for ~~data~~an entry read from the memory during a writeback cycle to write the read ~~data~~entry back to the memory.

36. (Canceled).

37. (Currently amended) The medium of claim 35, wherein the first group of ~~computer~~executable instructions includes executable instructions to store ~~metadata information~~usage bits for data in a destructive read memory.

38. (Canceled).

39. (Canceled).

40. (Canceled).

41. (Canceled).

42. (Currently amended) An apparatus comprising:

a non-volatile destructive read memory to cache data for a storage device and to store usage bits to indicate usage information for the cache data stored in the non-volatile destructive read memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods,

wherein ~~usage information~~a usage bit is updated during a writeback cycle to rewrite ~~data~~a corresponding entry destroyed during a read ~~process~~from the non-volatile destructive read memory back to the non-volatile destructive read memory.

43. (Previously presented) The apparatus of claim 42, wherein the non-volatile destructive read memory is a polymer ferroelectric random access memory (PFRAM), a magnetic RAM (MRAM), or a core memory.

44. (Previously presented) The apparatus of claim 42, wherein the storage device is a magnetic or optical memory device.

45. (Currently amended) The apparatus of claim 42, ~~further~~ comprising:
a cache controller coupled to the non-volatile destructive read memory; and
a main memory coupled to the cache controller.

46. (Previously presented) The apparatus of claim 42, wherein the non-volatile destructive read memory is a polymer ferroelectric memory.

47. (Canceled).

48. (Previously presented) The apparatus of claim 42, wherein the usage information is least recently used information.

49. (Previously presented) The memory of claim 12, wherein the destructive read memory is a non-volatile memory.

50. (Canceled).

51. (Currently amended) An apparatus comprising:
memory to store data and usage bits to indicate usage information for ~~data~~entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods,

wherein ~~usage information~~a usage bit for ~~data~~an entry read from the memory is to be updated during a writeback cycle to write the read ~~data~~entry back to the memory.

52. (Previously presented) The apparatus of claim 51, wherein the memory comprises cache memory.

53. (Previously presented) The apparatus of claim 51, wherein usage information comprises least recently used information.

54. (Previously presented) The apparatus of claim 51, wherein the memory comprises destructive read memory.

55. (Previously presented) The apparatus of claim 51, wherein the memory comprises non-volatile memory.

56. (Canceled).